Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Original) A method of fabricating a transistor having a source, drain, and a gate on a substrate, the method comprising:

implanting, into a surface of the substrate, a first impurity region (500A) with a first volume and a first surface area, the first impurity region being of a first type;

implanting, into a source region of the transistor, a second impurity region (518) with a second volume and a second surface area in the first surface area of the first impurity region, the second impurity region being of an opposite second type relative to the first type;

forming a gate oxide (508) between the source region and a drain region of the transistor, the gate oxide of the transistor being formed after implantation of the second impurity region;

covering the gate oxide with a conductive material (708A);

implanting, into the source region of the transistor, a third impurity region (514) with a third volume and a third surface area and a fourth impurity region (516) with a fourth volume and a fourth surface area, in the second surface area of the second impurity region, the third impurity region being of the first type, the fourth impurity region being of the opposite second type; and

implanting, into the drain region of the transistor, a fifth impurity region (510) with a fifth volume and a fifth surface area, the fifth impurity region being of the first type.

2. (Original) The method of claim 1, further comprising implanting, into the drain region of the transistor, a sixth impurity region (512) with a sixth volume and a sixth surface area in the first surface area of the first impurity region, the sixth impurity region being implanted with a spacing from the second impurity region, the sixth impurity region being of the first type.

3. (Original) The method of claim 2, wherein the sixth impurity region is self aligned to the gate of the transistor and is implanted after forming the gate of the transistor.

4. (Original) The method of claim 2, wherein the sixth impurity region is non-self aligned to the gate of the transistor and is implanted prior to forming of the gate of the transistor.

5. (Original) The method of claim 2, wherein the sixth impurity region is a double doped drain implant (1604).

6. (Original) The method of claim 2, wherein the sixth impurity region is a conventional CMOS well implant, the CMOS well implant being of the first type.

7. (Original) The method of claim 2, wherein the spacing of the second impurity region from the sixth impurity region is sized such that the sixth impurity region is spaced a predetermined distance (d) away from the gate of the transistor as measured along a surface of the transistor.

8. (Original) The method of claim 2, wherein the first impurity region and the sixth impurity region are implanted using a same mask.

9. (Original) The method of claim 2, wherein the implantation of the fifth impurity region is defined by a slit mask, the fifth impurity region forming multiple implants (1812) spaced apart relative to each other along a surface of the transistor in the drain region of the transistor.

10. (Original) The method of claim 9, wherein the third impurity region, the fifth impurity region and the sixth impurity region are implanted simultaneously using the slit mask.

11. (Original) The method of claim 1, wherein implanting the second impurity region includes implanting the second impurity region using a first implant (802) and a second implant (804).

12. (Previously presented) The method of claim 11 , wherein the first implant is a high energy implant.

13. (Previously presented) The method of claim 11, wherein the first implant is a large angle tilt implant.

14. (Original) The method of claim 1, further comprising implanting, into the source region of the transistor a seventh impurity region (1704) with a seventh volume having a seventh surface area, and implanting, into the drain region of the transistor, an eighth impurity region (1706) with an eighth volume having an eighth surface area, the seventh impurity region and the eighth impurity region being of the first type.

15. (Original) The method of claim 1, further comprising:
forming a field oxide (2702) on the drain region of the transistor.

16. (Original) The method of claim 1, wherein the transistor is an LDMOS transistor.

17. (Previously presented) A method of fabricating an LDMOS transistor, the method comprising:

implanting, into a source region of the LDMOS transistor, a P-body;

forming a gate oxide for the LDMOS transistor, the gate oxide for the LDMOS transistor being formed after implantation of the P-body of the LDMOS transistor; and

implanting, into the source region of the LDMOS transistor, an n+ region to provide an ohmic contact, the n+ region being located within the P-body.

18. (Original) The method of claim 17, wherein implanting the P-body includes implanting the P-body using a first implant (802) and a second implant (804).

19. (Original) The method of claim 18, wherein the first implant is a high energy implant.

20. (Original) The method of claim 18, wherein the first implant is a large angle tilt implant.

21-22. (Cancelled)

23. (New) The method of claim 18, wherein the second implant is implanted over the first implant, wherein the second implant is operable to control a channel length of the LDMOS transistor.

24. (New) The method of claim 18, further comprising fabricating at least one CMOS transistor using a sub-micron CMOS process.

25. (New) The method of claim 24, wherein the first implant controls a vertical doping profile of the source region without disrupting thermal budget of the sub-micron CMOS process.

26. (New) The method of claim 24, wherein the second implant controls a lateral doping profile of the source region without disrupting thermal budget of the a sub-micron CMOS process.